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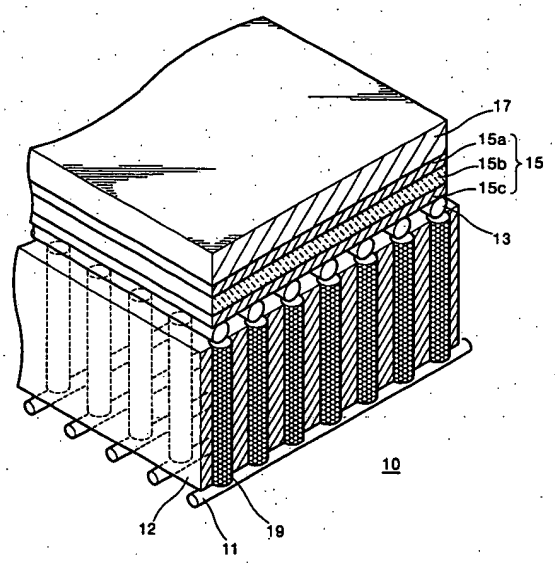
(54) Memory device utilizing vertical nanotubes

(57) A memory device using vertical nanotubes is provided. The memory device includes an array of first electrodes in strips, a dielectric layer, an array of nanotubes, an array of second electrodes in strips, a memory cell, and a gate electrode. The dielectric layer is deposited on the first electrode array and has a plurality of holes. The nanotube array contacts the first electrode array, grows vertically through the holes of the dielectric layer, and emits electrons. The second electrode array contacts the nanotube array, and the second electrodes are arrayed on the dielectric layer perpendicular to the first electrodes. The memory cell is positioned on the second electrode array and traps electrons emitted from the nanotube array. The gate electrode is deposited on the upper surface of the memory cell and forms an electric field around the nanotube array. Accordingly, the memory device is highly integrated and has a large capacity.

FIG. 1



EP 1 435 660 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a memory device, and more particularly, to a memory device utilizing vertical nanotubes.

2. Description of the Related Art

[0002] Semiconductor nonvolatile memory devices are basically comprised of a transistor which serves as a switch for securing a current path and a floating gate which preserves electric charges between gates.

[0003] To make much current flow in a transistor, the transistor must have a high transconductance (unit: gm) property. Accordingly, there is a recent trend that a metal oxide field effect transistor (MOSFET) with a high transconductance property is used as a switch in a semiconductor memory device.

[0004] MOSFETs are basically comprised of a control gate formed of doped polycrystalline silicon and a source region and a drain region which are formed of doped crystalline silicon.

[0005] Under a certain voltage condition, the transconductance of a MOSFET is inversely proportional to the length of a channel and the thickness of a gate oxide film and directly proportional to a surface mobility, the permittivity of the gate oxide film, and the width of the channel. Because the surface mobility and the permittivity of the gate oxide film are pre-determined by materials, that is, silicon for a wafer, silicon oxide for the gate oxide film, etc., a high transconductance can only be secured by increasing a ratio of the with to length of the channel or decreasing the thickness of the gate oxide film.

[0006] To manufacture highly-integrated memory devices, the size of a MOSFET must be reduced by downsizing the control gate, the source region, and the drain region. This downsizing creates several problems.

[0007] For example, a reduction in the size of the control gate causes a reduction in the cross-sectional area of the control gate, such that large electrical resistance may occur in the MOSFET. A reduction in the size of the source and drain regions causes a reduction in their thicknesses, that is, in their junction depths and accordingly causes larger electrical resistance. Also, a reduction in the distance between the source and drain regions causes a punch through where a depletion layer in the source region contacts a depletion layer in the drain regions occurs, making it impossible to control current. Such a reduction in the size of a memory device reduces the width of a channel to 30nm or less and accordingly disrupts a smooth flow of current to make the memory device malfunction. Because conventional memory devices having Si MOSFETs have the above-described problems when integration density increases, there is a limit in achieving highly-integrated memory devices.

SUMMARY OF THE INVENTION

[0008] The present invention provides a highly-integrated memory device having a large capacity by using vertically-grown carbon nanotubes.

[0009] According to an aspect of the present invention, there is provided a memory device using vertical nanotubes. The memory device includes an array of first electrodes in strips, a dielectric layer, an array of nanotubes, an array of second electrodes in strips, a memory cell, and a gate electrode. The dielectric layer is deposited on the first electrode array and has a plurality of holes arranged in the dielectric layer. The nanotube array contacts the first electrode array, vertically grows through the holes of the dielectric layer, and emits electrons. The second electrode array contacts the nanotube array, and the second electrodes are arrayed on the dielectric layer perpendicular to the first electrodes. The memory cell is positioned on the second electrode array and traps electrons emitted from the nanotube array. The gate electrode is deposited on the upper surface of the memory cell and forms an electric field around the nanotube array.

[0010] The first electrodes are source electrodes, and the second electrodes are drain electrodes.

[0011] The nanotubes are carbon nanotubes.

[0012] The memory cell includes a first insulation film formed below the gate electrode, a second insulation film deposited on the second electrode array, and a charge storage film interposed between the first and second insulation films and trapping charges emitted from the nanotube arrays.

[0013] The first and second insulation films are formed of aluminum oxide.

[0014] The charge storage film is formed of silicon or silicon nitride.

[0015] The charge storage film may be formed of silicon nano quantum dots.

[0016] Preferably, the length of each of the nanotubes is 5-10 times greater than the width of each of the second electrodes.

[0017] Preferably, the gate electrode is 5-10 times wider than the second electrodes.

[0018] Preferably, the memory cell has a thickness of about 30nm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a perspective view of a memory device according to a first embodiment of the present invention;
FIG. 2 is a perspective view of a memory device according to a second embodiment of the present invention;
FIG. 3 is a conceptual diagram for illustrating a principle in which electrons are trapped in a memory cell in the memory device according to the first embodiment of the present invention of FIG. 1;
FIG. 4 shows equipotential curves in the memory device according to the first embodiment of the present invention when a predetermined voltage is applied to gate electrodes, which are arranged at intervals over drain electrons;
FIG. 5 is a graph showing the distribution of an electric field around drain electrodes in the memory device according to the first embodiment of the present invention; and
FIG. 6 is a graph briefly showing the results of a simulation of the memory device according to the first embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] A memory device using nanotubes according to the present invention will now be described more fully with reference to the drawings, in which embodiments of the invention are shown.

[0021] FIG. 1 is a perspective view of a memory device 10 according to a first embodiment of the present invention. Referring to FIG. 1, the memory device 10 includes an array of source electrodes 11, a dielectric layer 12, an array of carbon nanotubes 19, an array of drain electrodes 13, a memory cell 15, and a gate electrode 17. The source electrodes 11 are arrayed in one direction. The dielectric layer 12 is formed on the array of source electrodes 11 and has a plurality of nano-holes arranged in a pattern. The array of carbon nanotubes 19 is vertically grown from the array of source electrodes 11 through the nano-holes of the dielectric layer 12. The drain electrodes 13 are arrayed in a direction perpendicular to the direction in which the source electrodes 11 are arrayed, such as to cross the carbon nanotubes 19 at right angles. The memory cell 15 contacts the upper surfaces of the drain electrodes 13. The gate electrode 17 is deposited on the memory cell 15.

[0022] The source electrode array and the drain electrode array are formed using a metal deposition technique. To be more specific, titanium (Ti) is deposited to a thickness of about 10nm on a substrate, gold (Au) is deposited to a thickness of about 50nm on the titanium film, and the resulting substrate is partially lifted off such as to obtain the source and drain electrodes 11 and 13.

[0023] The dielectric layer 12 is generally formed using an anodic aluminum oxide (AAO) process. In an AAO process, while aluminum is being anodized and turned into alumina, a plurality of nano-holes are formed in a material layer. The nano-holes are generally arranged such as to make a hexagonal honeycomb shape, but may be arranged in a square shape by using a mask or the like. The nano-holes shown in FIG. 1 are arranged in a square shape.

[0024] The carbon nanotubes 19 are vertically grown through the nano-holes of the dielectric layer 12 using a chemical vapor deposition (CVD) method. Using the CVD method, multi wall nanotubes are formed. The multi wall nanotubes can be of a metal type or a semiconducting type depending on the conditions of the CVD method. The carbon nanotubes 19 serve as channels through which electrons move. Nanotubes other than the carbon nanotubes 19 can be used if they have similar properties to the carbon nanotubes 19.

[0025] The memory cell 15 includes a first oxide film 15a, a nitride film 15b, and a second oxide film 15c that are sequentially stacked. The first and second oxide films 15a and 15c serve as insulation films and are usually formed of silicon oxide (SiO_2). The nitride film 15b is generally formed of silicon nitride and can store information by capturing electrons, which are moved by the potential of an electric field, because the nitride film 15b has a structure in which dangling bonding can occur. The memory cell 15 can be deposited to a thickness of several tens of nm using a CVD method.

[0026] The gate electrode 17 is formed of a metal or a semiconductor. A predetermined voltage is applied to the gate electrode 17 to control the flow of electrons that move through the carbon nanotubes 19. When the voltage is applied to the gate electrode 17, an electric field is formed under the gate electrode 17, and electrons are emitted from the source electrodes 11 to the drain electrodes 13 via the carbon nanotubes 19 in a Fowler-Nordheim manner and move opposite to the direction of the electric field toward the memory cell 15. The electrons are stored in the nitride film 15b, which serves as an electron storage film, and the number of stored electrons can be controlled by varying the intensity of the voltage applied to the gate electrode 17.

[0027] FIG. 2 is a perspective view of a memory device 20 according to a second embodiment of the present invention. Referring to FIG. 2, the memory device 20 is the same as the memory device 10 of FIG. 1 except that they have memory cells of different structures. A memory cell 25 in the memory device 20 includes an electron storage film 25b formed of nano quantum dots between first and second insulation films 25a and 25c. The first and second insulation films 25a and 25c can be formed of oxide, for example, silicon oxide.

[0028] Here, the nano quantum dots are usually formed of silicon using a physical or chemical technique. The physical technique may be a vacuum synthesis technique, a gas-phase synthesis technique, a condensed phase synthesis technique, a fast deposition technique using an ionized cluster beam, a consolidation technique, a fast milling technique, a mixalloy processing technique, a deposition technique, or a sol-gel technique. The chemical technique includes a general CVD technique and a technique of coating a core material with a different material.

[0029] The nano quantum dots are formed to be several nm in size so that they can easily trap several to several tens of electrons. As the sizes of nano quantum dots decrease, the number of electrons trapped in the nano quantum dots may decrease, and accordingly the voltage applied to the gate electrode 17 may become lower.

[0030] FIG. 3 is a conceptual diagram for illustrating a principle in which electrons are trapped in the memory cell 15 in the memory device according to the first embodiment of the present invention of FIG. 1. Referring to FIG. 3, when a predetermined voltage is applied between the source and drain electrodes 11 and 13, electrons move to the drain electrodes 13 along the carbon nanotubes 19. When a positive voltage higher than the voltage applied between the source and drain electrodes 11 and 13 is applied to the gate electrode 17, an electric field E is emitted from the gate electrode 17 in the directions indicated by dotted lines. When the voltage applied to the gate electrode 17 becomes equal to or higher than a threshold voltage Vth, some electrons moving toward the drain electrodes 13 along the carbon nanotubes 19 move opposite to the direction of the electric field E and is directed toward the memory cell 15. As the voltage applied to the gate electrode 17 increases, the number of electrons moving opposite to the direction of the electric field E increases, and the number of electrons trapped in the nitride film 15b of the memory cell 15 increases. The trapping of electrons in the memory cell 5 is called a programming process.

[0031] An erasing process is achieved by emitting the electrons stored in the nitride film 15b of the memory cell 15 by reversing the original direction of the electron field E by applying to the gate electrode 17 a voltage having opposite polarity to voltage applied during programming.

[0032] The memory devices according to the above-described embodiments of the present invention can achieve a maximum electron storage efficiency by controlling the width (w) of a gate electrode and the width (t) of drain electrodes with respect to the length (l) of carbon nanotubes. Preferably, the memory device can be manufactured so as to have a maximum electron storage efficiency of 1:w=1:1, 1:t=5:1, or 1:t=10:1.

[0033] FIG. 4 shows equipotential curves in the memory device according to the embodiment of the present invention when a predetermined voltage is applied to the gate electrode 17 disposed a predetermined distance apart from the upper surface of the drain electrodes 13. Here, the voltage applied to the gate electrodes 17 is 10V.

[0034] In FIG. 4, variation in electric potential can be seen from the pattern of equipotential curves. The value of the electric potential increases from blue equipotential curves to red equipotential curves. Since the direction of the electric field is perpendicular to the equipotential curves, the electric field is directed to the gate electrode 17. Since the initial kinetic energy of electrons emitted from carbon nanotubes is near "0", the electrons are moved by the electric field. Hence, the electrons are directed to the gate electrode 17. The distribution of electrons depends on the distribution of an electric field between the gate electrodes 17 and the drain electrodes 13.

[0035] FIG. 5 is a graph showing the distribution of an electric field around drain electrodes in the memory device according to the first embodiment of the present invention. The drain electrodes 13 are positioned in an area (D) ranging from 1.75 to 2.25, and the electric field at the area (D) is 5×10^5V/cm at most. As shown in FIG. 5, the intensity of the electric field decreases as distance from the area (D) of the drain electrodes 13, the area (D) ranging between 1.75 and 2.25 in the X axis. Also, as shown in FIG. 5, the electric field at part of an area (A) ranging from 1.5 to 2.5, defined by excluding a part screened by the drain electrodes 13 from the area (A), is relatively high, that is, 2×10^5 to 5×10^5V/cm. In other words, it can be guessed from these simulation results that a strong electric field is distributed around the drain electrodes 13, and accordingly, many electrons are moved around the drain electrodes 13.

[0036] FIG. 6 is a graph diagrammatically showing variation in a source-drain current Isd with respect to a gate voltage (Vg), according to the results of a simulation of the memory device according to the first embodiment of the present invention. In the simulation, the gate electrode 17 is 100nm×100nm in size, a driving voltage of about 1 GHz is applied to the gate electrode 17, current of 50nA is emitted from the carbon nanotubes 19, and the interval between the gate electrode 17 and the drain electrodes 13 is about 30nm. For convenience, it is assumed that all emitted electrons are trapped in the memory cell 15.

[0037] If a positive gate voltage V_g is applied when the source-drain current is 0, the value of the source-drain current starts to increase in a direction P. At this time, electrons move through the carbon nanotubes 19. At V_{g1}, electrons start to be emitted from the carbon nanotubes 19, and the source-drain current Isd continuously increases. At a gate voltage higher than V_{g1}, the memory cell 15 can perform programming. When a gate voltage of V_{g2} is applied, electrons stored

in the memory cell 15 reach a saturation state. Therefore, even when a gate voltage of V_{g2} or greater is applied, electrons are screened by the pre-stored electrons, and thus no further increase of the source-drain current Isd occurs.

[0038] To erase data recorded in the memory cell 15, the gate voltage V_g is reduced. Although the gate voltage V_g is reduced, emission of electrons is screened by the electrons pre-stored in the memory cell 15 until the gate voltage V_g is decreased to V_{g3}, and accordingly, no decrease of the source-drain current Isd occurs. When the applied gate voltage V_g becomes smaller than V_{g3}, the source-drain current Isd starts to decrease in a direction Q. Even when the gate voltage V_g becomes 0, the source-drain current Isd does not become zero due to the flow of electrons pre-stored in the memory cell 15 but flows until the gate voltage V_g is decreased to a certain negative value.

[0039] The charge (Q) of electrons emitted from the carbon nanotubes 19 is calculated from the current (I) emitted from the carbon nanotubes 19 and the driving frequency ($f=1/\Delta T$), which are both pre-set in the above-described simulation, as expressed in Equation 1:

$$Q = I \cdot \Delta T = 50 \cdot 1/2 \cdot 10^{-9} = 2.5 \times 10^{-7} \text{ Coulomb} \quad (1)$$

[0040] A capacitance (C) between the gate electrodes 17 and the drain electrodes 13 is calculated to be about 1.18×10^{-17} F using Equation 2:

$$C = \varepsilon\frac{A}{d} = 3.54 \times 10^{-11} \times \frac{10^{-7} \times 10^{-7}}{3 \times 10^{-8}} = 1.18 \times 10^{-17} \text{ F} \quad (2)$$

wherein the dielectric constant (ε) of the oxide films of the memory cell 15 is approximated to be about 4.

[0041] A threshold voltage Vth is calculated to be about 2.1V by substituting Equations 1 and 2 into Equation 3:

$$V_{th} = \frac{Q}{C} = \frac{2.5 \times 10^{-17}}{1.18 \times 10^{-17}} = 2.1V \quad (3)$$

[0042] It can be seen from the magnitude of Vth being 2.1V that the memory device according to the first embodiment of the present invention has excellent memory characteristics.

[0043] The present invention provides a memory device in which electrons emitted from vertical carbon nanotubes are trapped in a memory cell, thereby achieving a highly-integrated large-capacity memory device.

[0044] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims. For example, carbon nanotubes can be grown in shapes other than the shapes mentioned herein.

Claims

1. A memory device (10, 20) using vertical nanotubes, the memory device comprising:

   an array of first electrodes (11) in strips;

   a dielectric layer (12) deposited on the first electrode array (11) and having a plurality of holes arranged in the dielectric layer;

   an array of nanotubes (19) contacting the first electrode array, vertically growing through the holes of the dielectric layer, and emitting electrons;

   an array of second electrodes (13) in strips which contact the nanotube array (19) and are arrayed on the dielectric layer perpendicular to the first electrodes (11);

   a memory cell (15, 25) positioned on the second electrode array and trapping electrons emitted from the nanotube array (19); and

a gate electrode (17) deposited on the upper surface of the memory cell (15, 25) and forming an electric field around the nanotube array (19).

2. The memory device (10, 20) of claim 1, wherein the first electrodes (11) are source electrodes, and the second electrodes (13) are drain electrodes.

3. The memory device (10, 20) of claim 1 or 2, wherein the nanotubes (19) are carbon nanotubes.

4. The memory device (20) of claim 1, 2 or 3, wherein the memory cell (25) comprises:

a first insulation film (25a) formed below the gate electrode;

a second insulation film (25c) deposited on the second electrode array (13); and

a charge storage film (25b) interposed between the first and second insulation films (25a, 25c) and trapping charges emitted from the nanotube arrays (19).

5. The memory device of claim 4, wherein the first and second insulation films (25a, 25b) are formed of aluminum oxide.

6. The memory device of claim 4 or 5, wherein the charge storage film (25b) is formed of one of silicon and silicon nitride.

7. The memory device of claim 4 or 5, wherein the charge storage film (25b) is formed of silicon nano quantum dots.

8. The memory device of one of the claims 1 to 7, wherein the length of each of the nanotubes is 5-10 times greater than the width of each of the second electrodes.

9. The memory device of one of the claims 1 to 8, wherein the gate electrode is 5-10 times wider than the second electrodes.

10. The memory device of one of the claims 1 to 9, wherein the memory cell (15, 25) has a thickness of about 30nm.

FIG. 1

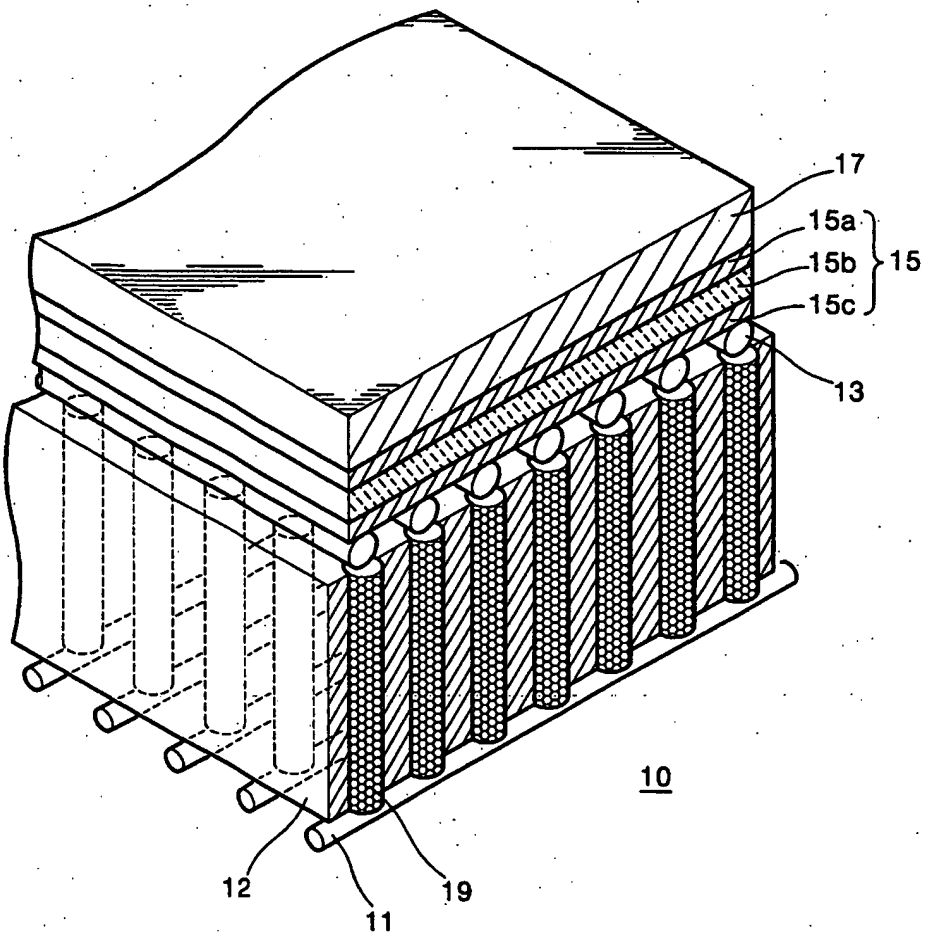


FIG. 2

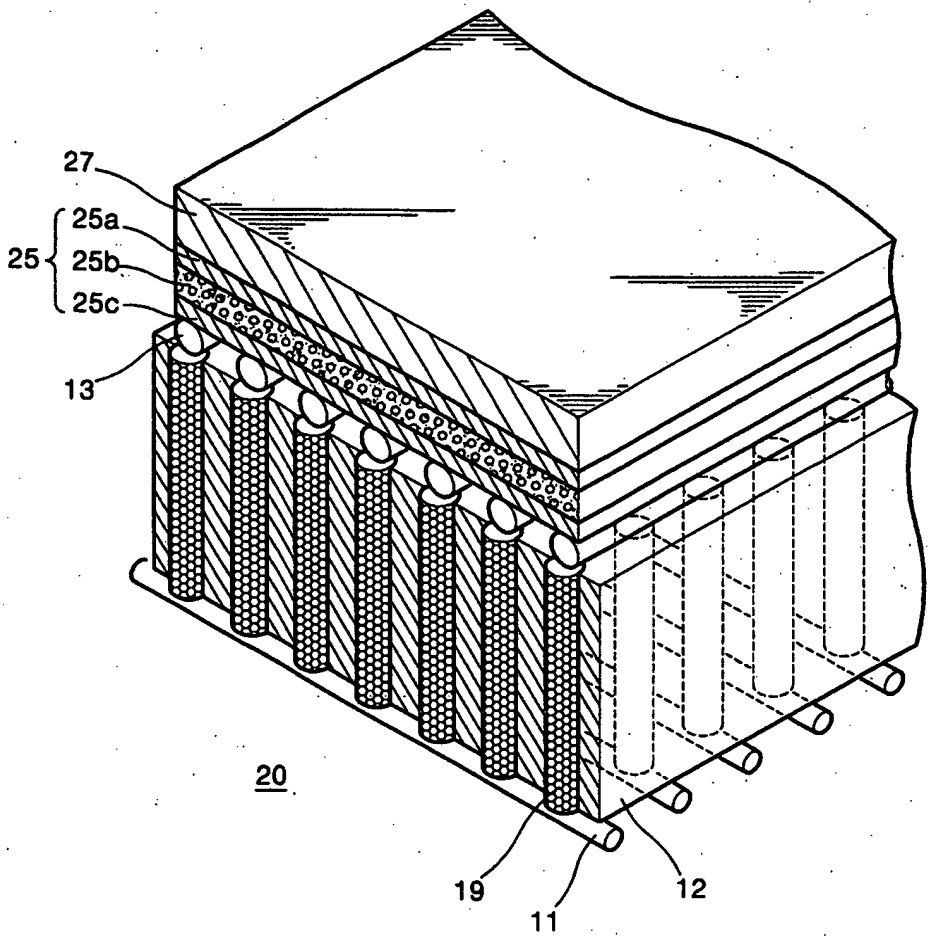


FIG. 3

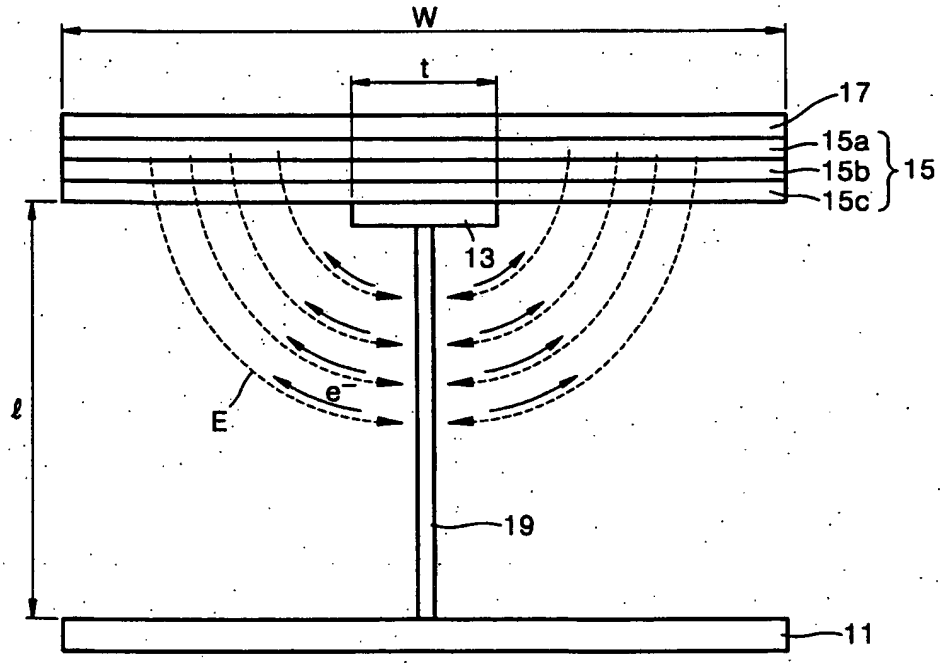


FIG. 4

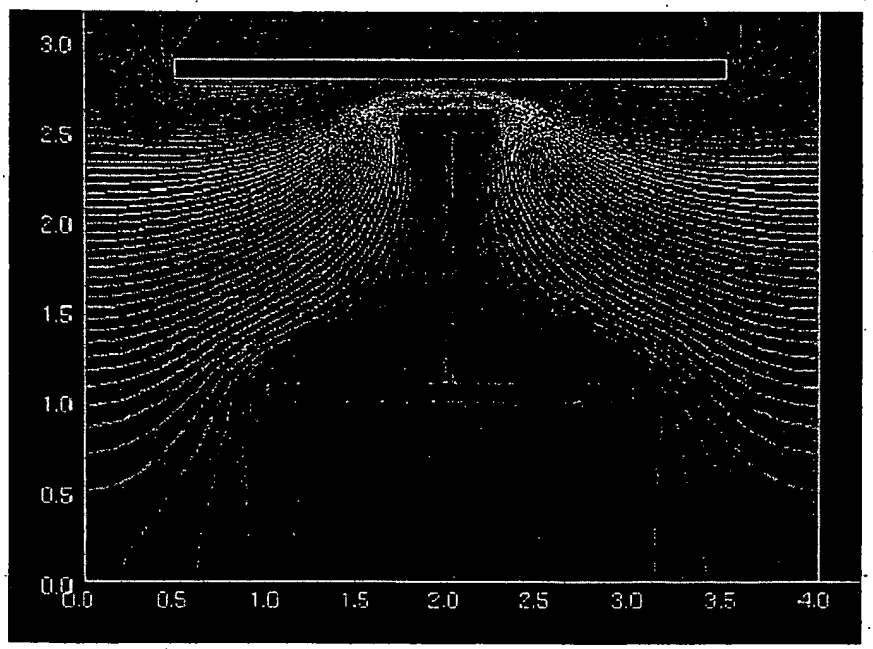


FIG. 5

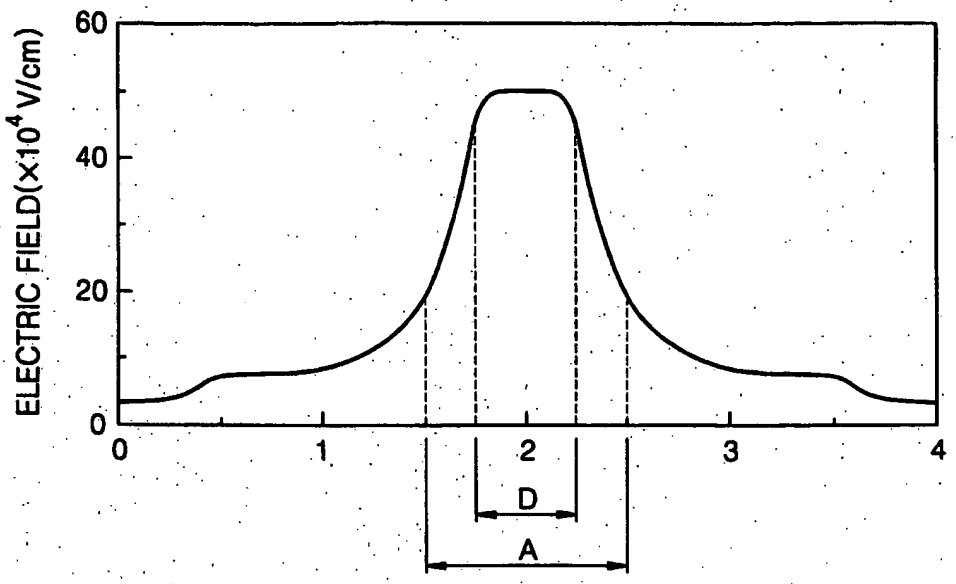
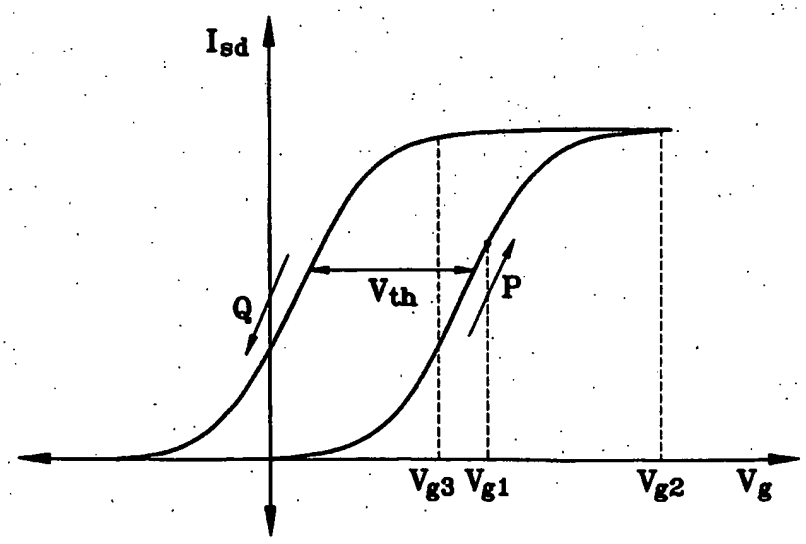

ELECTRIC FIELD(×10^4 V/cm)
60
40
20
0
0
1
2
3
4
D
A

FIG. 6


Isd
Q
Vth
P
Vg3
Vg1
Vg2
Vg